Introduction to the K5 System

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1. Concept of the K5 System

The K5 VLBI system is designed to perform real-time or near-real-time VLBI observations and correlation processing using Internet Protocol over commonly used shared network lines. Various components are being developed to realize the target goal in various sampling modes and speeds. The entire system will cover various combinations of sampling rates, number of channels, and number of sampling bits. All of the conventional geodetic VLBI observation modes will be supported as well as the other applications like single-dish spectroscopic measurements or pulsar timing observations will also be supported. The concept as the family of the K5 system is show in the Fig. 1.

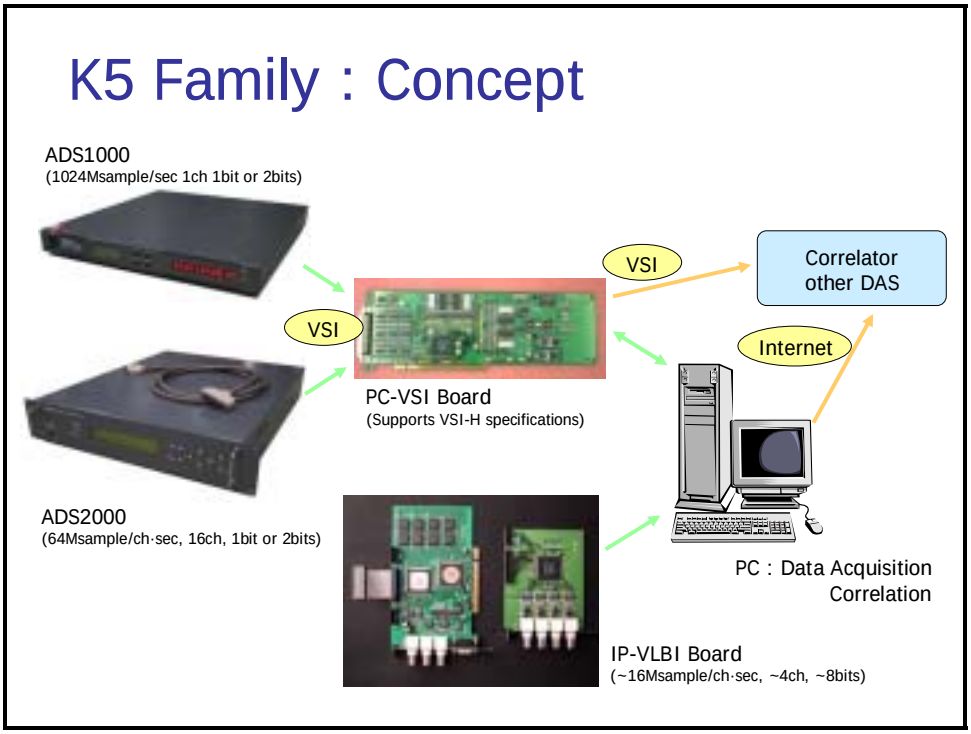

Fig. 1 Concept of the entire K5 System.

As shown in the Fig. 1, if the ADS1000 or ADS2000 sampler unis are used, the PC-VSI board is used to interface the VSI (VLBI Standard Interface) compliant signal from the sampler unit and the PCI bus of the PC. Both of the sampler units, ADS1000 and ADS2000, are equipped with two VSI compliant connectors which can support data rates up to 1024Mbps. In addition, ADS2000 unit supports 64MHz clock signaling specified as the option of the VSI specification to support the data rates up to 2048Mbps with a single

VSI connector. Whereas the ADS1000 is designed as a single channel high speed sampler unit, the ADS2000 is designed for geodetic VLBI observations by supporting 16 channels at the sampling rates up to 32Msps for each channel. When the ADS1000 or ADS2000 sampler unit is used, the PC-VSI board is connected with the sampler unit by using VSI specified data signaling. Although the function is not fully supported at present, the same PC-VSI board will be used to extract data from the K5 system by using VSI.

When relatively low sampling rates are required, PC systems with the IP-VLBI boards are used as shown in the bottom of the Fig. 1. The IP-VLBI board is consist of a main board and a daughter board, and it occupies two board slots in the PCI bus of the PC system. Each board is equipped with four BNC connectors from which the base-band signal is supplied and sampled at the Nyquist frequency of the signal. In this configuration, A/D sampling capability is embedded in the board and the PC can be directly connected to the base band converter units.

2. K5/VSSP System

Fig. 2 shows the evolution of the VLBI observation and data processing systems developed at the Kashima Space Research Center of the National Institute of Information and Communications Technology (NICT). The K5 system is characterized by the use of conventional PC systems. The data correlation will be performed on the PC systems using software correlator programs. Similarly, the K4 system can be characterized by the use of rotary-head, cassette type magnetic tape recorders, and the K3 system can be characterized by the use of open-reel magnetic tape recorders.

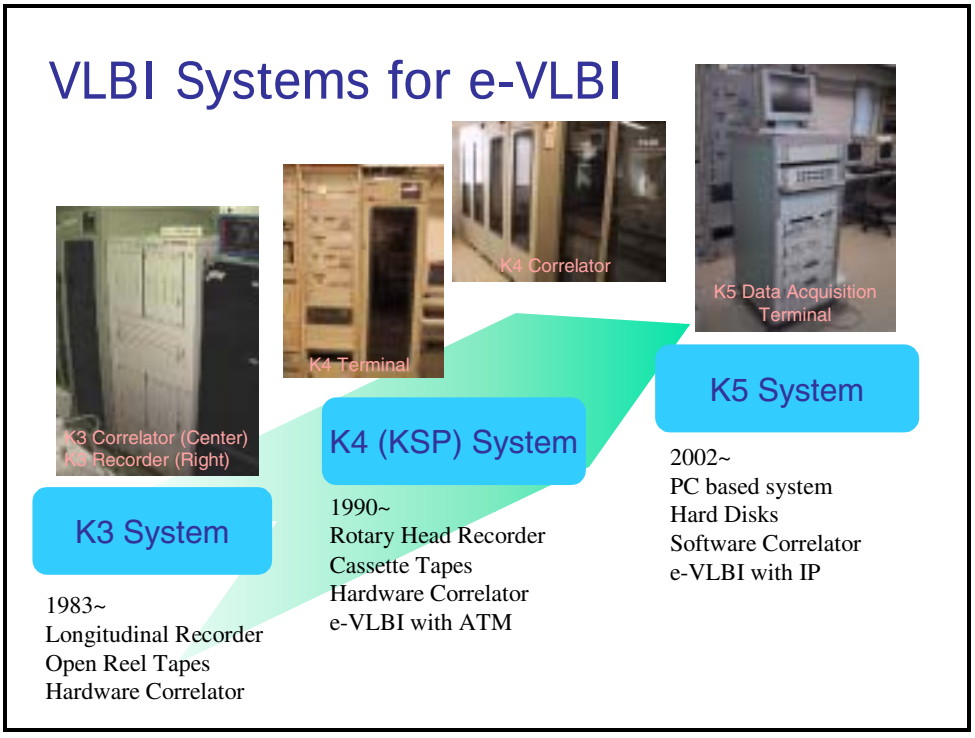

Fig. 2 Developments of K3, K4 and K5 VLBI systems.

Fig.3 is one of the combined set of the K5 system and it is specified as the K5/VSSP system. VSSP is an acronym of the Versatile Scientific Sampling Processor. This name is used because the system is designed to be used for general scientific measurements. The system has a capability to sample analog data stream by using the external frequency standard signal and the precise information of the sampled timing. The system is also used to process the sampled data. For geodetic VLBI observations, software correlation program runs on the K5/VSSP system. Therefore, it can be said that the functions of the formatter, the data recorder, and the correlator are combined into the single system. It is consist of four UNIX PC systems. Each UNIX PC system has one IP-VLBI data sampling board on its PCI interfacing bus. Table 1 shows the specifications of the K5/VSSP system. Each board can sample 4 channels of base-band signals at various sampling rates ranging from 40kHz to 16MHz. The timing of the sampling is controlled by the externally provided 10MHz and 1PPS reference signals so that precise timing information can be reproduced from the sampled data. Quantization bits can be set from 1, 2, 4, and 8. Because the board has these many sampling modes, it has many possibilities to be used not only for VLBI observations but also for various other scientific researches which require precise timing information in the data. Device driver software of the board has been developed on LINUX, FreeBSD, and Windows2000 operating systems, and FreeBSD is used in the K5/VSSP data acquisition terminals. Four PC systems are mounted in the lower part of the 19-inch standard rack. A signal distributor unit for 1-PPS and 10 MHz signals and 16-channel base-band signal variable amplifier unit are mounted in the upper part of the rack. The LCD monitor and the keyboard on the top of the rack are connected to the four PC systems by using a four-way switch. Each PC system is equipped with four removable parallel ATA 3.5 inch hard disk drives. The sampled data can be transferred to the network by using TCP/IP protocol or can be recorded to internal hard disks as ordinary data files. The maximum recording speed is currently restricted by the speed of the CPU and the speed of the PCI internal bus. Currently, the total recording speed of 512 Mbps has been achieved. To process the data sampled with the K5 data acquisition system, software correlation processing program is also under development on conventional PC systems. The correlation processing program receives data from K5 data acquisition systems over the network using TCP/IP protocol and then calculates cross correlation functions without any specially designed hardware. It can also read data files on internal hard disks. These capabilities allow to transfer observed data in real-time if the connecting network is fast enough, or in near real-time if data buffering is required. Since easily re-writable software programs and general PC systems are used, the processing capacity and the function of the correlator can be easily expanded and upgraded. Fig. 4 shows the schematic diagram of the data flow of the K5 system.

Table 1. Specifications of the K5/VSSP system

Reference Signals	10MHz (+10dBm) and 1PPS
Number of Channels	16
A/D bits	1, 2, 4, or 8
Sampling Frequency (for each channel)	40kHz, 100kHz, 200kHz, 500kHz, 1MHz, 2MHz, 4MHz, 8MHz, or 16MHz
Maximum Data Rate	512Mbps

Fig. 3 Picture of the K5/VSSP system.

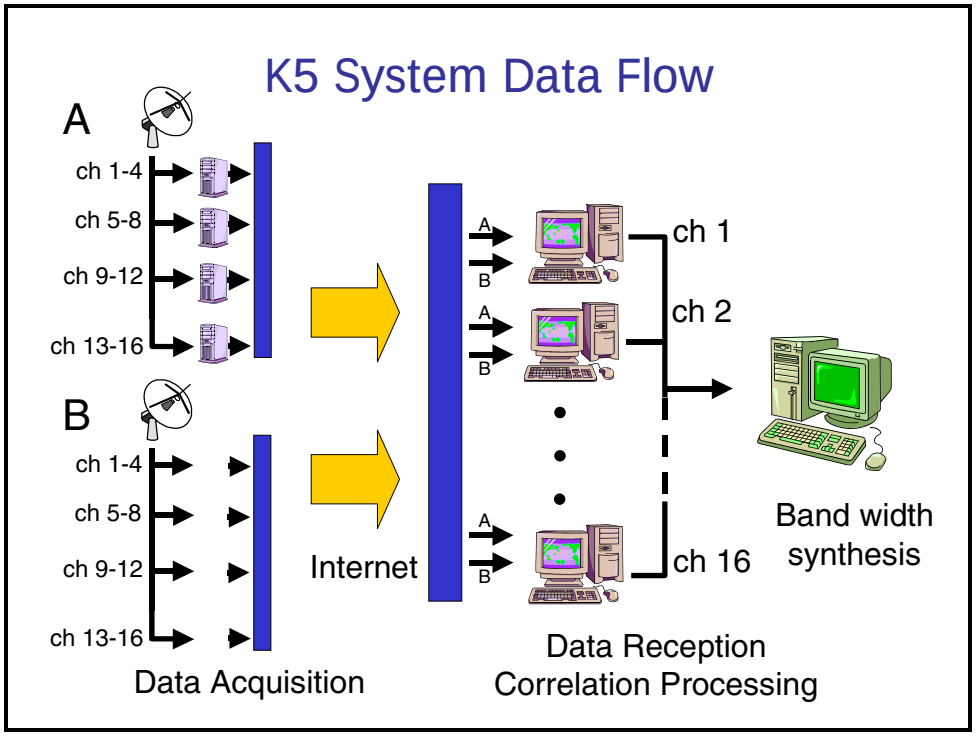

Fig. 4 Data flow of the K5/VSSP system in typical geodetic VLBI observations.

Appendix 1. List of utilities used with the K5/VSSP system

command	function
pctimeset	Adjust the time of PC system.
signalcheck	Check the presence of external 1PPS and 10MHz signals.
timedisp	Display the time set on the board
timesettk	Set the time on the board and synchronize the clock to the external 1PPS signal.
timesinc	Synchronize the clock on the board.
monit	Display histogram of the input signal(s).
skdchk	Read the schedule file and calculates necessary disk storage.
autoobs	Start data acquisition according to the schedule file.
sampling	Record single scan of data and generate a recorded data file.
datachk	Read the recorded data file and check whether any data were lost within each data segment.
extdata	Read the recorded data file and extract the data in the ASCII format.
datacut	Split the recorded data file.
four2one	Generate one channel data file from the recorded data file with four channels of input.
speana	Calculates power spectrum and display the results from recorded data file.
adbitconv	Change the sampling bits in the recorded data file.
one2four	Combine four recorded data files with one channel of input for each file, and generates a data file with four channels of input.
data_half	Convert the sampling data rate half of the original file.
data_double	Convert the sampling data rate double of the original file.

K5/VSSP (IP-VLBI) Board Data Format

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1 Introduction

The K5/VSSP (IP-VLBI) board is capable to sample either 1 channel or 4 channels of analog input with one of the quantization levels of 1 bit, 2 bits, 4 bits, or 8 bits. Sampling frequency can be set from 40kHz, 100kHz, 200kHz, 500kHz, 1MHz, 2MHz, 4MHz, 8MHz, or 16MHz. Sampled data can be stored to a data file on an internal hard disk drive. In addition, the data can be sent to the network interface by using UDP/IP or TCP/IP. In the following section, the data format of the data file created by the IP VLBI board is described.

2 Data structure

A data file contains sampled data for certain amount of time obtained by one IP VLBI board. The data file begins with a header section (HD) of the length of 64 bits and then 1 second of data stream is written in the sampling data section (SD) following the header section. This sequence repeats until the scan of the observation finishes as shown in the Table 1. The data format of each data section is described in the following subsections.

Header section (HD)	Sampling data section (SD)	HD	· ·
64 bits	40000 - 64000000 bits	64 bits	· ·

Figure 1: Data structure of the data file

2.1 Header section data format

A header section consists of 32 bits of HD1 and 32 bits of HD2. In the HD1 section, all bits are 1. In the HD2 section, time stamp and sampling information are written with the format explained in the Table 2.

2.2 Sampling data section

Data format of the sampling data section is described with the first 64 bits in the Tables 3 through 10.

Table 1: Data format of the header section

HD1 (32bits)

D0	(LSB)	Sync pattern (32 bits)
:		[FF FF FF FF]
D31	(MSB)	

HD2 (32 bits)

D0	(LSB)	Time (time of day) (17 bits)
:		(0〜86399 sec)
D16		elapsed time from 00h00m00s in seconds
D17		Index of the number of channels 0:1ch 1:4ch
D18		Index of sampling frequency (4 bits)
:		(Note: definitions for more than a 32MHz sampling are to support
:		the conversion from other format data such as Mark5)
:		0: 40kHz / 1: 100kHz / 2: 200kHz / 3: 500kHz
:		4: 1MHz / 5: 2MHz /6: 4MHz / 7: 8MHz / 8: 16MHz
:		9: 32MHz / 10: 64MHz / 11: 128MHz / 12: 256MHz / 13: 512MHz
D21		14: 1024MHz / 15: 2048MHz
D22		Index of the number of quantization (2 bits)
D23		0: 1 bit / 1: 2 bits / 2: 4 bits / 3: 8 bits
D24		Sync pattern 2 (8 bits)
:		[8Bh]
D31	(MSB)	

Table 2: Sampling data section data format (1 ch / 1 bit sampling)

1 ch / 1 bit sampling		
1st 32bits data		
D0	(LSB)	1st data (1bit)
D1		2nd data (1bit)
:		:
D31	(MSB)	32nd data (1bit)
2nd 32bits data		
D0	(LSB)	33rd data (1bit)
D1		34th data (1bit)
:		:
D31	(MSB)	64th data (1bit)
:		

Table 3: Sampling data section data format (1 ch / 2 bits sampling)

1 ch / 2 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (2bits LSB)
D1		1st data (2bits MSB)
D2		2nd data (2bits LSB)
D3		2nd data (2bits MSB
:		:
D31	(MSB)	16th data (2bits MSB)
2nd 32bits data		
D0	(LSB)	17th data (2bits LSB)
D1		17th data (2bits MSB)
D2		18th data (2bits LSB)
D3		18th data (2bits MSB)
:		:
D31	(MSB)	32th data (2bits MSB)
:		

Table 4: Sampling data section data format (1 ch / 4 bits sampling)

1 st / 4 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (4bits LSB)
:		:
D3		1st data (4bits MSB)
D4		2nd data (4bits LSB)
:		:
D7		2nd data (4bits MSB)
:		:
D31		8th data (4bits MSB)
2nd 32bits data		
D0	(LSB)	9th data (4bits LSB)
:		:
D31		16th data (4bits MSB)
:		

Table 5: Sampling data section data format (1 ch / 8 bits sampling)

1 ch / 8 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (8bits LSB)
:		:
D7		1st data (8bits MSB)
D8		2nd data (8bits LSB)
:		:
D15		2nd data (8bits MSB)
:		:
D31		4th data (8bits MSB)
2nd 32bits data		
D0	(LSB)	5th data (8bits LSB)
:		:
D31		8th data (8bits MSB)
:		

Table 6: Sampling data section data format (4 ch / 1 bit sampling)

4 ch / 1 bit sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (1bit)
D1		Ch.2 1st data (1bit)
D2		Ch.3 1st data (1bit)
D3		Ch.4 1st data (1bit)
D4		Ch.1 2nd data (1bit)
D5		Ch.2 2nd data (1bit)
:		:
D31	(MSB)	Ch.4 8th data (1bit)
2nd 32bits data		
D0	(LSB)	Ch.1 9th data (1bit)
D1		Ch.2 9th data (1bit)
:		:
D31	(MSB)	Ch.4 16th data (1bit)
:		

Table 7: Sampling data section data format (4 ch / 2 bits sampling)

4 ch / 2 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (2bits LSB)
D1		Ch.1 1st data (2bits MSB)
D2		Ch.2 1st data (2bits LSB)
D3		Ch.2 1st data (2bits MSB)
D4		Ch.3 1st data (2bits LSB)
D5		Ch.3 1st data (2bits MSB)
D6		Ch.4 1st data (2bits LSB)
D7		Ch.4 1st data (2bits MSB)
D8		Ch.1 2nd data (2bits LSB)
D9		Ch.1 2nd data (2bits MSB)
:		:
D31	(MSB)	Ch.4 4th data (2bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 5th data (2bits LSB)
D1		Ch.1 5th data (2bits MSB)
D2		Ch.2 5th data (2bits LSB)
D3		Ch.2 5th data (2bits MSB)
:		:
D31	(MSB)	Ch.4 8th data (2bits MSB)
:		

Table 8: Sampling data section data format (4 ch / 4 bits sampling)

4 ch / 4 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (4bits LSB)
:		:
D3		Ch.1 1st data (4bits MSB)
D4		Ch.2 1st data (4bits LSB)
:		:
D7		Ch.2 1st data (4bits MSB)
D8		Ch.3 1st data (4bits LSB)
:		:
D11		Ch.3 1st data (4bits MSB)
D12		Ch.4 1st data (4bits LSB)
:		:
D15		Ch.4 1st data (4bits MSB)
D16		Ch.1 2nd data (4bits LSB)
:		:
D19		Ch.1 2nd data (4bits MSB)
:		:
D31		Ch.4 2nd data (4bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 3rd data (4bits LSB)
:		:
D31		Ch.4 4th data (4bits MSB)
:		

Table 9: Sampling data section data format (4 ch / 8 bits sampling)

4 ch / 8 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (8bits LSB)
:		:
D7		Ch.1 1st data (8bits MSB)
D8		Ch.2 1st data (8bits LSB)
:		:
D15		Ch.2 1st data (8bits MSB)
D16		Ch.3 1st data (8bits LSB)
:		:
D23		Ch.3 1st data (8bits MSB)
D24		Ch.4 1st data (8bits LSB)
:		:
D31		Ch.4 1st data (8bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 2nd data (8bits LSB)
:		:
D31		Ch.4 2nd data (8bits MSB)
:		