IAA Correlator Center

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Abstract

The prototype correlator of ARC was produced. It is a 2-station VSI-H XF-type hardware VLBI correlator connected to two Mark 5B terminals. The fullscale 6-station VLBI correlator ARC is scheduled next and will be constructed soon.

The VLBI data of the 3-station sessions of the Russian national network Quasar was processed using the MicroPARSEC correlator.

1. Introduction

The IAA Correlator Center is located and staffed by the Institute of Applied Astronomy in St.-Petersburg, Russia.

The IAA Correlator Center is devoted to processing geodetic, astrometric, and astrophysical observations made with the Russian national VLBI network Quasar.

2. Summary of Activities

Development of the basic parts of the VLBI hardware XF Astrometric Radiointerferometric Correlator (ARC) was completed in 2008. The first prototype correlator was built.

The ARC hardware construction allows the formation of different scales of correlators, from single-baseline 2-station up to 15-baseline 6-station correlators, with 16 frequency channels in each baseline.

The ARC handles two-bit VLBI signals with a 32 MHz maximal TAC frequency. The maximal data range from each station is 1 Gbps. The ARC requires VSI-H input VLBI signals. It is equipped with Mark 5B playback terminals. The ARC hardware includes a Base Module of Correlator, Signal Distribution and Synchronization System, and standard computer and communication units.

The main part of the ARC is called the Base Module of Correlator (BMC). This device carries out all the hardware data processing. The BMC enables the processing of 16 single-baseline frequency channels of typical geodetic VLBI observations. The BMC contains 16 correlation units which are single-baseline single-channel XF correlators for calculating 64 complex delays and picking phase-cal tones. The BMC is based on FPGA technology. The data processing algorithms are implemented as FPGA firmware. The BMC is a Compact PCI 6U front plug-in board. It contains 34 FPGA, 32 RAM chips and a PCI controller chip.

The Signal Distribution and Synchronization System (SDSS) distributes signals from Mark 5B to BMC, so that each BMC receives signals from two Mark 5B terminals. In addition, the SDSS generates and sends synchronization signals DPSCLOCK and DPS1PPS to Mark 5B terminals. The SDSS has several types of Compact PCI boards in its constructions: Generator of Synchronization Signals, Signal Distribution Module, and Interface Module of Correlator.

The Generator of Synchronization Signals (GSS) produces DPSCLOCK and DPS1PPS signals and passes these to the Mark 5B terminals.

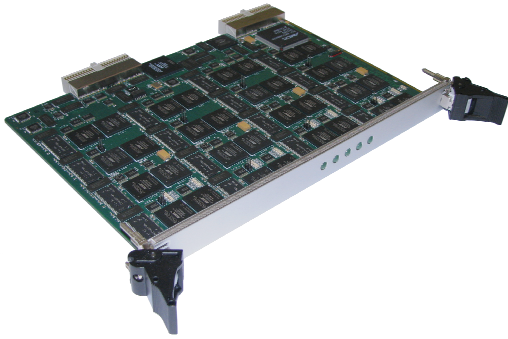The main part of data stream distribution is performed by Signal Distribution Modules (SDM).
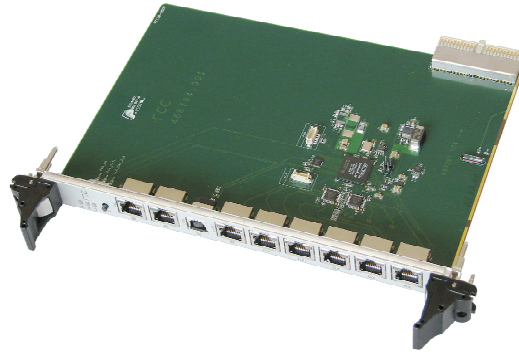
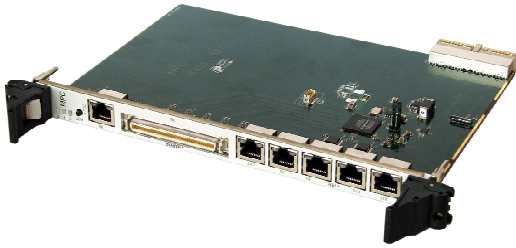Figure 1. BMC device.
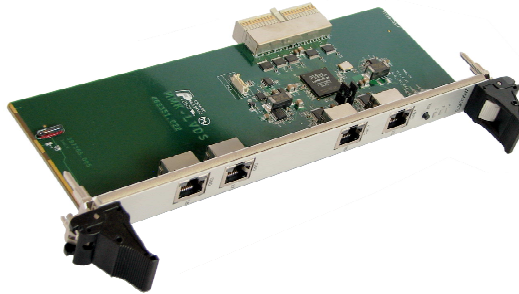

Figure 2. GSS device.

Figure 3. SDM device.

Figure 4. IMC device.

Up to five copies (for a 6-station correlator) of the Mark 5B output data streams from each of the Mark 5B terminals are produced by the SDM and then sent to the IMC.

The Interface Module of Correlator (IMC) receives 2 serial data streams coming from 2 SDMs, and transfers these to the BMC.

The SDM and GSS are the Compact PCI 6U front plug-in boards. The IMC is the Compact PCI 6U rear panel I/O board. The BMC, GSS, SDM and IMC modules are shown in Figs. 1, 2, 3, 4.

During 2008 the first prototype correlator of the ARC family was produced. It was built as a 2-station correlator, and a series of geodetic VLBI observations was performed to test this correlator in determining UT1-UTC. The prototype consists of two Mark 5B terminals, a Compact PCI 6U crate (Fig. 5) with BMC, GSS, two SDM and IMC modules, local network commutator, and PC.

The prototype hardware control is performed from the PC, which is connected to the crate through the correlator's local network. The correlator software is a distributed system between the PC and crate. The software is executed on Linux.

Fullscale ARC production started at the end of 2008. The goal for the 6-station 15-baseline correlator is the processing of all data from the national VLBI sessions. (At present this task is performed with the 12-board MicroPARSEC correlator.) We are planning to complete the 6-station ARC in 2009.
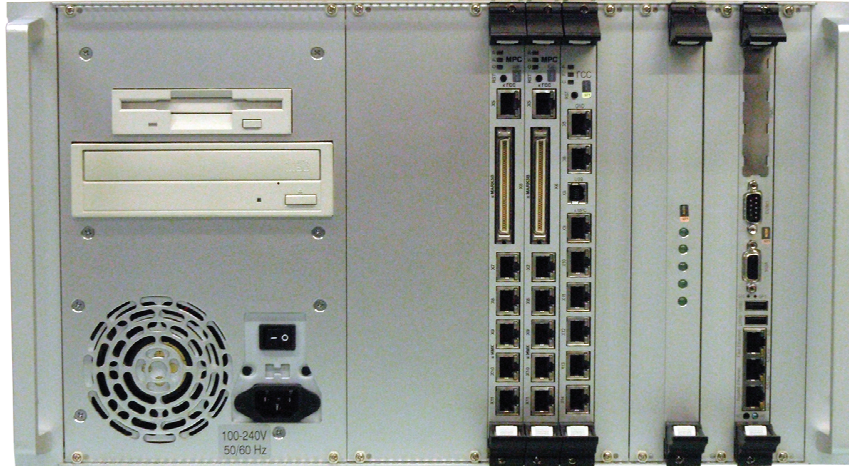
Figure 5. Compact PCI 6U crate.

3. Experiments Done

The regular national VLBI observations with the 3-station Quasar VLBI network were continued in 2008. Observational data were processed using the 12-board MicroPARSEC correlator. A total of twenty 24-hour and sixteen 8-hour VLBI sessions were processed. The resulting group and ionospheric delay accuracy varies from 50 to 100 picoseconds.

4. Staff

- Igor Surkis — leading investigator, software developer;

- Artemy Fateev — software developer;

- Alexey Melnikov — software developer, scheduler;

- Vladimir Mishin — software developer, post processing;

- Violet Shantyr — software developer, post processing;

- Vladimir Zimovsky — hardware developer.