

# Haystack Observatory Technology Development Center

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**Abstract** Technology development at MIT Haystack Observatory focused on three areas in 2013:

- Mark 6
- RDBE 3.0
- KPGO 20-m VGOS Receiver Upgrade

## 1 Mark 6 High Speed Data Recorder

In 2013, the development and the implementation of the Mark 6 recording system continued. The software can now record up to four 2 Gb/s Mark 5B streams, which are converted on the fly to vdif datastreams differentiated by thread ID. A single 8 disk module in good health is able to record that 8 Gb/s datarate, or slightly less. Given that the Mark 6 has a  $\sim 60$  GB ram buffer, the fifo allows scans of several minute duration to be captured in this mode, so long as there is some time between scans for draining the fifo. Using the nominal 2-module/16-disk configuration, the full datastream can be recorded continuously. Similarly, a 16 Gb/s input data rate can be captured for short periods in two modules (= 16 disks), although for continuous recording four modules should be used.

Manufacture of the Mark 6 was transferred to Conduant Corp., and they began filling orders mid-year. The software is open source, and it is available on the Haystack website. In addition to the Mark 6 control software, there are various utilities there to allow for data quality assessment, as well as interim conver-

sion software for use at correlators. A python program called RM6\_CC allows for control of the hardware via an XML schedule. Multiple test observation sessions were held, employing Mark 6s at the Westford and GGAO antenna sites.

## 2 RDBE Version 3.0

Development of a new RDBE firmware version 3.0 was initiated in 2013. The RDBE v3.0 is an operations-oriented personality that represents an enhancement to the RDBE v1.4 personality. The version 3.0 personality incorporates a number of operations and diagnostic capabilities that include the following:

- Integrated 1PPS Delay Measurement
- Pulse Calibration Extraction
- 1PPS-triggered raw ADC capture
- Arbitrary test vector injection

In addition to these features, the v3.0 firmware represents a complete re-engineering of the v1.4 PFB firmware code. This new development simplified the firmware signal processing and has been verified against the theoretical PFB algorithm implemented in a MATLAB model. The verification process ensures that the RDBE v3.0 signal processing that is implemented on the Xilinx FPGA IC is performing the correct operations, and it is anticipated that a test vector procedure will be incorporated to verify field installations of the RDBE running this personality. This verification process is conducted by introducing a known digital test vector at the frontend (input) port of the FPGA, recording the resultant output 2-bit samples generated by the FPGA operations, and

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directly comparing (differencing) the RDBE output samples to the theoretical sample values computed by the MATLAB model.

As part of the v3.0 firmware development, the RDBE server software, which interprets commands from an external RDBE user, was rewritten to incorporate the additional firmware features that are available in the v3.0 firmware. As part of the re-write, the complexity was reduced from approximately 50,000 lines of code to approximately 4,000 lines.

The server software also captures VLBI-critical diagnostic data on each 1PPS pulse, packages the data into a multicast network packet, and transmits the data over the 1 GigE network interface for reception by any client listening on the designated network port. This diagnostic data includes the current UT time as maintained by the RDBE firmware as well as the delay offsets of this clock relative to the RDBE operating system clock (i.e., server clock), the GPS 1PPS signal, and the MASER 1PPS signal. Also contained in this multicast packet are the samples of the pulse calibration signal as reconstructed by the pulse calibration extraction feature and the first 4,000 samples of the 8-bit frontend ADC samples as triggered by the RDBE 1PPS.

The server also provides an information-rich numerical and graphical output data display that is intended to provide feedback to the RDBE user. This graphical display updates on each 1PPS pulse and plots the ADC raw capture samples with the associated histogram and spectrum. This display also plots the reconstructed pulse calibration signal and the noise diode on and off accumulator counts for each PFB frequency channel. Figure 1 displays an example of the RDBE server's graphical output display.

### 3 KPGO 20-m VGOS Receiver Upgrade

In 2013, Haystack Observatory developed and fabricated a VGOS receiver frontend upgrade for the KPGO 20-m radio telescope. Diagrams of the new receiver frontend are shown in Figure 2. The receiver enclosure, which is identical in design to the existing S/X KPGO 20-m receiver enclosure, was provided by NASA/Excelsis and was recovered from a decommissioned/damaged NASA radio telescope. Haystack refurbished the receiver enclosure and developed a full 3D mechanical design in the CAD software suite

SolidWorks. This mechanical model also serves as electronic documentation for the KPGO site personnel and can be viewed by downloading a free SolidWorks viewer available at the software vendor's website.

Similar to previous Haystack broadband receiver frontend designs, the KPGO frontend incorporates a customized QRFH feed. This feed was optimized for the 0.43 focal-length-to-diameter ratio characteristic of the KPGO 20-m optics. Receive pattern measurements of the cryogenic frontend demonstrate that the expected broadband aperture efficiency of the KPGO 20-m VGOS system should be approximately 50% over the 2 to 14 GHz frequency range as shown in Figure 3. The measured noise temperature of the new 20-m VGOS receiver frontend is shown in Figure 4. Based on these noise temperature and aperture efficiency estimates, the SEFD of the KPGO 20-m telescope following the VGOS upgrade is expected to be approximately 900 Jy which is equivalent to that of the X-band section in the existing system. The VGOS receiver frontend upgrade for the KPGO 20-m antenna was delivered to Kokee Park in September 2013.

Presently, a failure in the KPGO 20-m frontend receiver "box" rail system is inhibiting removal of the S/X band receiver frontend section from the antenna. Installation of the VGOS frontend is awaiting mechanical refurbishment of this rail mechanism.

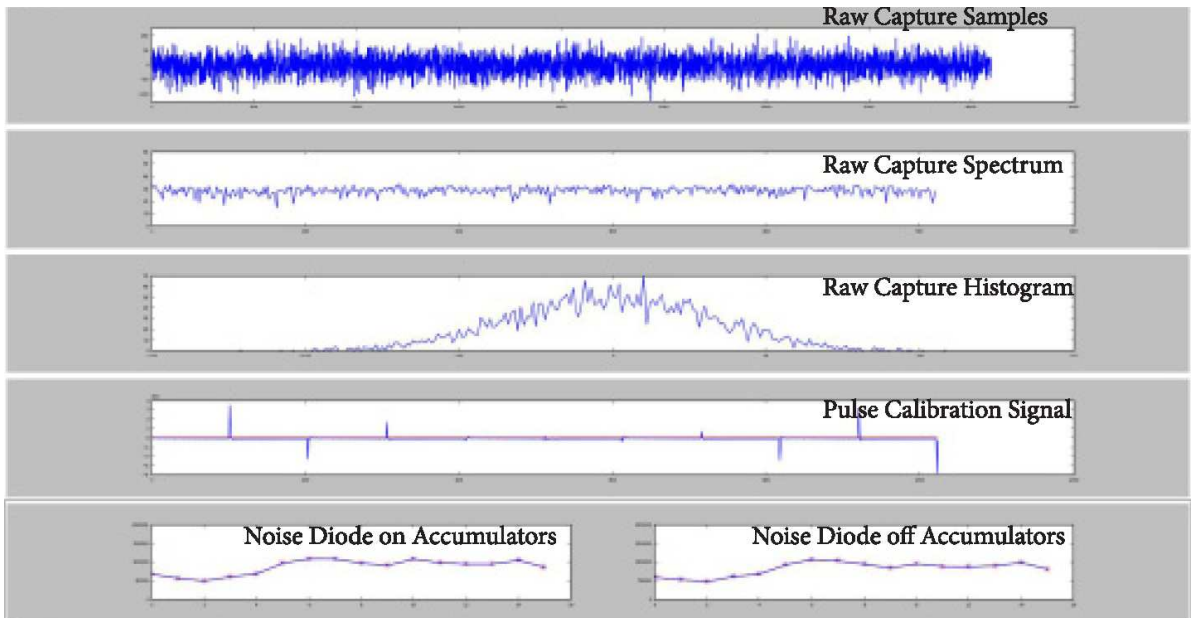


Fig. 1 Graphical output display generated by the RDBE v3.0.

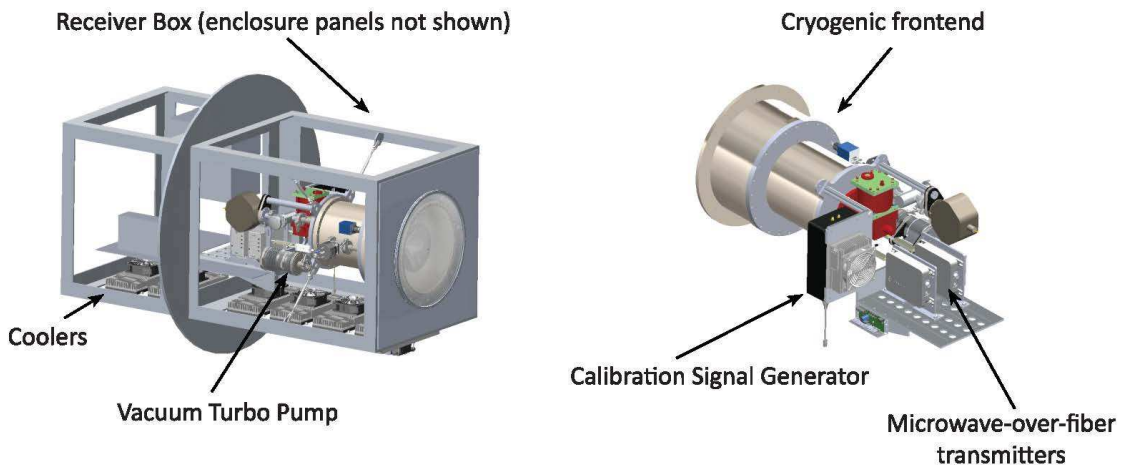
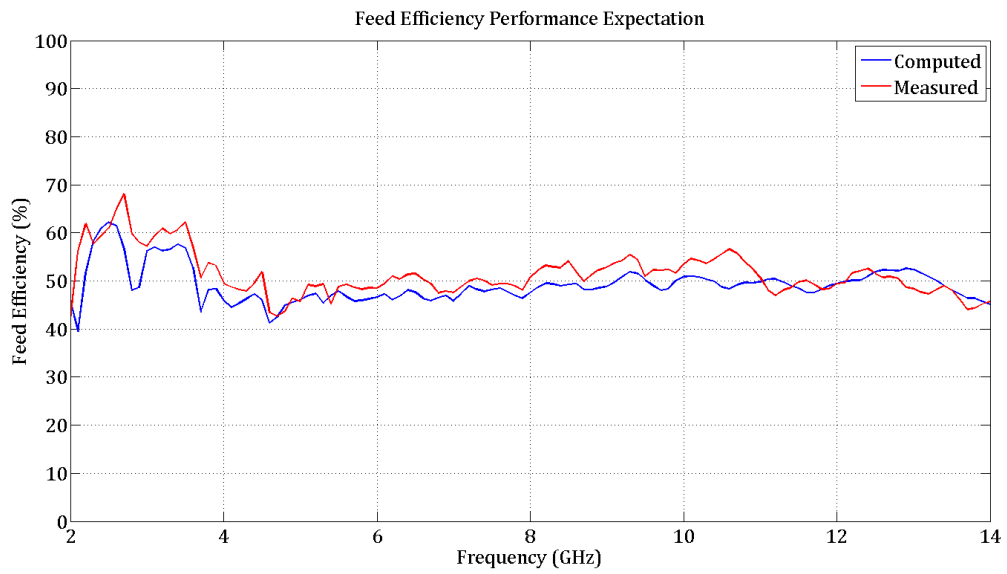
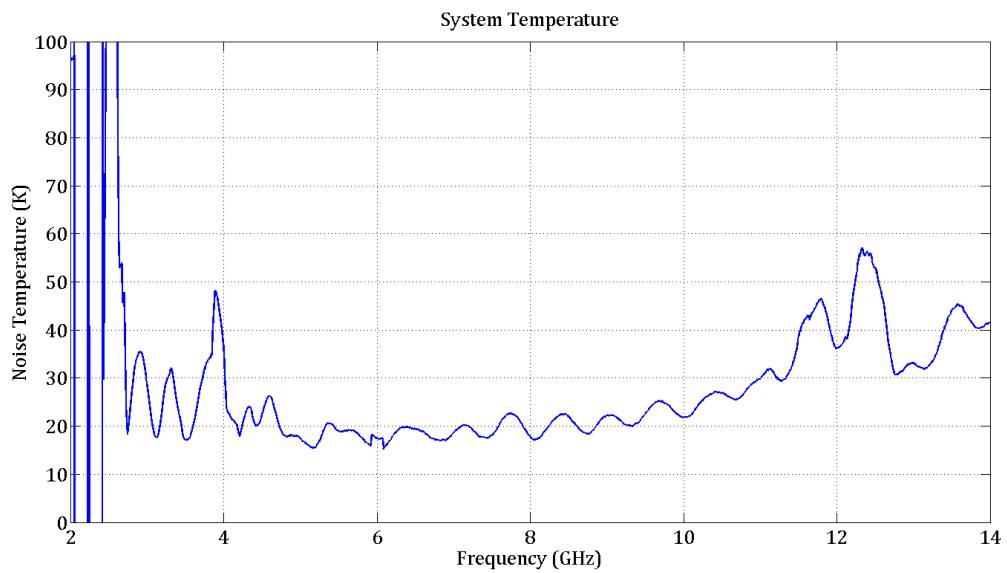


Fig. 2 KPGO 20-m VGOS receiver frontend upgrade.



**Fig. 3** Expected aperture efficiency of the KPGO 20-m following the VGOS receiver frontend upgrade.



**Fig. 4** Noise temperature of the KPGO 20-m VGOS receiver frontend upgrade.