Using the Multifunctional Digital Backend System on Radio Telescopes of Svetloe Observatory

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Abstract The RT-32 and RT-13 VLBI radio telescopes of the Quasar network use various equipment for radio interferometric, radiometric, and spectral observations. The Data Acquisition Systems (DAS) currently used for Very Long Baseline Interferometry (VLBI) on the RT-32 telescopes at the Svetloe, Zelenchukskaya, and Badary observatories are narrow-band and do not fully meet modern requirements for the frequency bands of the recorded signals. The broadband DAS used on the RT-13 telescopes at the Badary and Zelenchukskaya observatories do not have sufficient functionality necessary to meet modern VGOS requirements. To solve these problems, the Institute of Applied Astronomy of the Russian Academy of Sciences (IAA RAS) has developed a Multifunctional Digital BackEnd system (MDBE) capable of replacing all the variety of DAS and other output devices used on the RT-13 and RT-32 radio telescopes.

Keywords Digital backend, Data Processing

1 MDBE Hardware Design

The task of a radio telescope backend is to capture the signals from receivers, make required processing with them depending on the type of observation being performed, and send the result to the recording system. The MDBE can contain up to 12 channels, or Digital Signal Processing (DSP) units, implementing this task with all output of the receiver. Each DSP unit contains a 10-bit analog-to-digital converter (ADC) digitizing the signal from the receiver, Field Programmable Gate Arrays (FPGAs) processing the digitized signal, and optical transceivers transmitting the output data to the recorder (Figure 1).

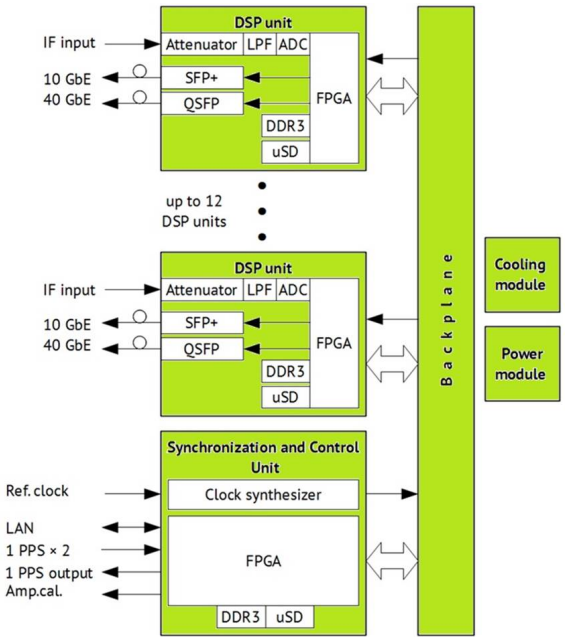

Fig. 1 MDBE Structure: DSP – digital signal processing unit, LPF – low-pass filter, ADC – analog-to-digital converter, IF – intermediate frequency signal, FPGA – field-programmable gate array, QSFP and SFP+ – quad and enhanced small form-factor pluggable optical transmitters, 1PPS – one pulse per second signal, LAN – local area network, Amp. cal. – amplitude calibration control signal, DDR3 – double-data-rate synchronous dynamic random access memory, and μSD – micro SD flash card.

The ADC works with a sample rate of 4096 MHz and 2 GHz input bandwidth. This allows the direct digitization of signals of the intermediate frequency (IF)

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range coming from the receivers, which is either 100–1000 MHz for the RT-32 receiving system [1] or 1–2 GHz for the Tri-band [2] and ultra-wideband [3] receivers of the RT-13. The last modification of the ultra-wideband receiver has eight channels with an IF range from 50 MHz to 2 GHz. By using the MDBE, this allows observing in four bands located in a range from 3 to 16 GHz with a total recorded bandwidth of 8 GHz in each polarization, which gives a total data rate of 64 Gbps. The signal level of the DSP unit input can noticeably differ depending on the receiver type, the observing band, and the amount of radio-frequency interference (RFI) in the band. To prevent ADC saturation, the DSP unit contains a small analog frontend with a digital attenuator tuned in the range from 0 to 31.75 dB with a 0.25 dB step. The frontend also includes a low-pass filter to prevent aliasing from the second Nyquist zone. The FPGA captures the data stream from the ADC and performs signal processing, having onboard more than 400 thousands of flip-flops, 200 thousands of look-up tables, 900 DSP blocks, and an embedded dual-core ARM processor to implement all required DSP functions. By using embedded transceivers and SFP+ or QSFP modules, the output data are transmitted through fiber lines to the Recording and Data Buffering System [4]. One SFP+ module supports a 10 GbE link; that is enough for typical VLBI applications, using 2-bit quantization of output data. In case of need, an additional 40 GbE QSFP module allows transferring of the raw ADC data stream that can be used to implement even more sophisticated DSP algorithms in an external board or accelerator card. The DSP unit is implemented as the 14-layer printed circuit board (PCB), covered by a heat sink for heat removal and shielding noisy and sensitive parts of the circuit (Figure 2, shown without a heat sink).

Fig. 2 The DSP unit shown with the heat sink removed.

All DSP units are connected with the Synchronization and Control Unit (SCU) over a backplane. The SCU, based on the same FPGA as the one in DSP units, receives control commands through a 10/100/1000 Ethernet interface, either optical or copper, and communicates with all DSP units through dedicated 256 Mbps duplex links. The FPGA firmware of the SCU and DSP units can be loaded from the onboard microSD card or remotely over the network. Thanks to this, the developers can create perfectly tailored firmware for each observation mode and switch between them in seconds.

For clocking for all FPGAs and ADCs of the MDBE, the SCU contains a mezzanine module of a clock synthesizer that generates required signals. It accepts a 5, 10, or 100 MHz signal as a reference clock, normally from an H-maser. The generated clocks are distributed to all DSP units through aligned traces over highly stable clock distributors, located on the backplane. The resulting clock jitter measured from ADC clock input lies at the level of 250 femtoseconds and practically does not affect the signal-to-noise ratio of the digitized signals. Special care has been taken in the clock synthesizer design to ensure that the phases of generated clocks remain constant after resynchronization or a power reset. By this we keep constant the ADC clock phase that defines the position of sampling points in time and thus directly impacts the MDBE group delay. To indicate the first signal sample in a second, the SCU generates a special 1PPS (one pulse per second) signal and distributes it over all DSP units. The internal 1PPS signal can be synchronized by 1PPS coming from the observatory clock, and the delay between them is constantly measured.

To support continuous amplitude calibration, the SCU generates a control signal to switch on and off the calibration noise generator in the receiver. The frequency of the control signal can be set in a range from 2 Hz to 2 kHz. The SCU has identical PCB size and stackup, but the board is located in a covered cassette with a wider front panel to fit all required connectors (Figure 3).

The MDBE was originally designed to be installed inside the elevation cabin of the radio telescope, which simplifies the connection with the receivers and eliminates instabilities caused by transmission of sensitive analog signals over long coaxial or fiber lines through moving parts of the antenna's cable loops. The MDBE is based on a 19″ 3U Europac PRO chassis (Figure 4).

The chassis can fit one SCU and up to 12 DSP units that are inserted into the backplane along aluminum

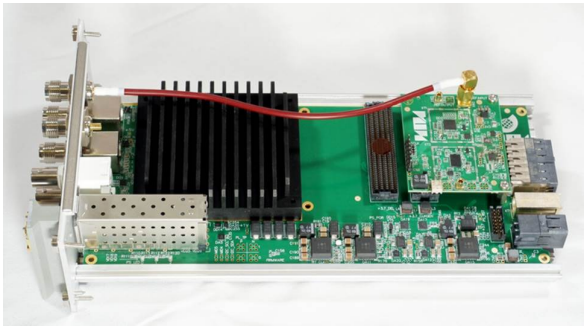

Fig. 3 MDBE Synchronization and Control Unit without a cover.

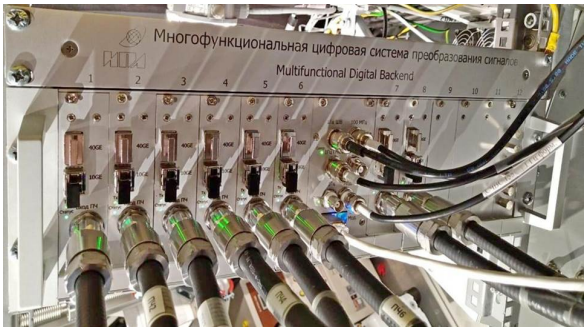

Fig. 4 The MDBE installed in the RT-13 radio telescope in the Svetloe observatory.

guide rails from the front side. Usage of the backplane and the guide rails makes the maintenance simple, as any unit can be easily replaced in a minute. To provide an adequate cooling of the system, there is a cooling module of 1U height, located above the main case. The module contains three regulated fans that are controlled by the SCU using a specialized three channel fan controller. All synchronization and control signals from the SCU pass to the DSP units through a backplane board. The SCU communicates with the DSP units through dedicated lines in the LVDS standard with a 256 Mbps data rate. The backplane includes distributors for the ADC and the FPGA clock signals, the 1PPS signal, and the ADC calibration signal.

2 MDBE Firmware Design

The data samples coming from the ADC have to be securely entered into the FPGA in correct order and without any glitches. The data samples come over four buses, and each consists of 10 data bits, an overrange flag, and an accompanying clock signal. The data rate of the coming samples is 1,024 MSPS per bus, which cannot be directly triggered by common FPGA resources because of operating frequency limits. To reduce the frequency the embedded deserializers are used, which convert input serial bit streams to a number of parallel streams with a respectively lower frequency, 256 MHz in our case. That gives totally 16 parallel samples of data on the output of the deserializer block, which further come to the downconverter block, where the main processing is performed. The block of downconverters cuts the interesting parts of the spectrum from the input band, shifts them to baseband, and filters them to form the required bandwidth. There is separate firmware created to implement either one 1,024 MHz channel or one 512 MHz channel or up to sixteen 32 MHz channels. The observations in wideband mode usually do not require fine frequency tuning in the backend, because the receiving system can tune frequencies with at least a 400 kHz step. In 1,024-MHz-bandwidth mode, the MDBE allows a choice between the ranges 0–1,024 MHz or 1,024–2,048 MHz. In 512-MHz-bandwidth mode the channel can be set anywhere in a range from 0 to 2,048 MHz with a 128 MHz step. For narrowband modes fine frequency tuning is required. The firmware supports a 10 kHz tuning step, which provides compatibility with legacy backends. The quantizer performs “requantization” of the samples from the downconverters to 2 bits, using the root mean square value of the signal as a threshold. The quantized samples come to the output stage that packs them into VDIF packets, forms Ethernet frames with the required upper-level headers (IP, UDP) and sends the resulting frames to the SFP+ transceiver. The output stage currently supports up to an 8,192 Mbps data rate through a single 10 GbE link. The VDIF formatter packs the input data stream into packets of the required size with a 32-byte header. The payload length can be set up to 8,192 bytes, which still fits to Jumbo frame limitations while simplifying recording of the data stream by reducing the number of packets per second. The Signal Analysis Functions combine several auxiliary blocks that are not directly involved in the signal path but are used to obtain various useful information about the signal. The overrange counter uses a special overrange bit of the ADC output buses to calculate the percentage of the ADC overflows. The ADC calibrator calculates the degree of discrepancy

between the samples received from the first and other ADC cores. The power meter is used to calculate the power of the samples received from the ADC. The PCAL extractor clears PCAL tones of noise, making them available for further analysis. The data exchange within the system is performed by a specially designed Control Link protocol, which is implemented in the FPGA. The communication protocol includes in each message a compact header containing the clock word, payload length, and message type. The integrity of the messages is monitored using a CRC32 checksum. The Direct Memory Access (DMA) controller provides a fast link between the Control Link and the allocated DDR3 memory area, allowing the processor to interrupt only when a message has been fully received and placed in memory or fully transferred from memory and sent. The control functions are implemented using the processing system based on an ARM Cortex-A9 processor. The program, written in C, performs the following functions:

- regularly reading onboard sensors and estimating the system health based on the values;
- setting the parameters implemented in the FPGA blocks and reading the required data from them;
- taking part in synchronization procedures;
- executing outside commands coming from the SCU itself or forwarded by the SCU from a remote host;
- receiving from the SCU new firmware and loading it;
- controlling internal registers of the SFP, the QSFP, and the ADC;
- other minor functions.

Currently the following VLBI modes are implemented in the DSP MDBE: Wideband 1024 MHz, Wideband 512 MHz, and VGOS mode with up to 16 channels with bandwidths of 32, 16, 8, 4, 2, and 0.5 MHz. The narrowband mode allows compatibility with "legacy" backends and allows the MDBE to be used to upgrade the RT-32 antenna. In addition, the MDBE firmware for single-dish modes for spectrometric observations [5] and radiometric observations with RFI rejection in the frequency domain is currently under active development. A more detailed description of the software and hardware implementation of the MDBE system can be found in [6]. The following are the main features.

3 Experimental Use of the MDBE

To test the compatibility of the MDBE with standard broadband systems, an experimental session of VLBI observations, r4121c, was conducted on April 30, 2020 based on Svetloe-Zelenchukskaya-Badary with the recording of signals in the 512 MHz wideband in the S and X frequency bands. As the result of processing the signals on the RASFX correlator, correlation responses with a signal-to-noise ratio (SNR) from 52.7 to 299 in the X-band and from 31.5 to 131.1 in the S-band were obtained for all sources (Figure 5). The values obtained are in good agreement with those predicted by theory.

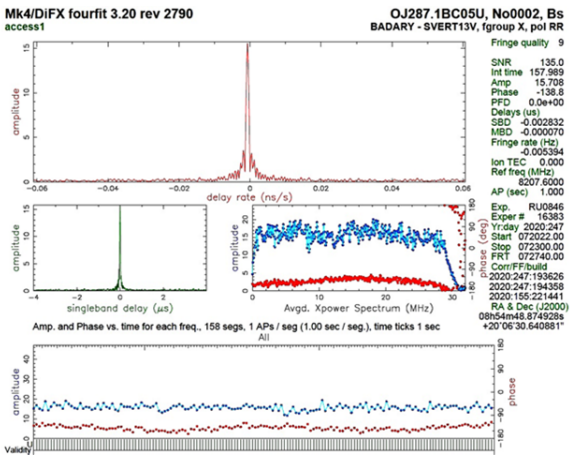

Fig. 5 An example of the correlation response from the OJ287 source in channel No. 9 during observations on the Svetloe–Badary radio interferometer using a narrow-band DAS and the MDBE.

The MDBE operation on the RT-13 radio telescope in the Svetloe observatory was checked during the international VLBI observing session R1972 of the IVS network on November 9, 2020. The IVS network operated with the standard geodesic frequencies set in the S- and X-bands and a sample of 16 frequency channels with 8 MHz width for each. For all 384 scans of observations in which the RT-13 radio telescope with MDBE participated, correlation responses with all foreign radio telescopes participating in the observations were registered.

In 2021 several experiments of radar observations of the Moon were carried out in the Svetloe Observatory. These experiments involved the 35-meter antenna

(DSA 3) to transmit and the RT-13 radio telescope to receive echoes from the Moon. The echo was recorded using the MDBE with 2-bit quantization in two separate channels in left and right circular polarizations. The system operated in the VGOS mode with 32 MHz bandwidth and 1,336 MHz in the IF band. The observation data were transmitted via high-speed optical communication lines from the observatory to the server of the IAA RAS Data Processing Center in St. Petersburg. As a result the power spectra of the echo signal reflected from the lunar crater "Archimedes" in left and right circular polarizations (Figure 6) and a radar image of the Moon at 4.2 cm wavelength [7] were obtained.

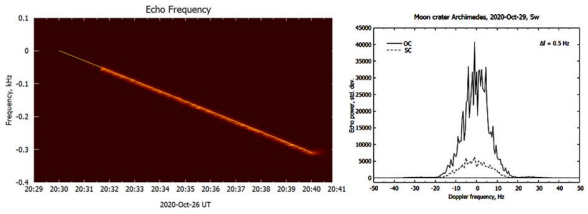

Fig. 6 Spectrogram and echo power spectra of the Moon obtained with the MDBE.

In December 2020, the MDBE was put into operation on the RT-13 radio telescope at the Svetloe Observatory. As part of the RT-13 equipment, the MDBE participated in all regular VLBI observations to determine UT1-UTC. From December 2020 more than 1,000 sessions of VLBI observations under the "R" program in the S- and X-bands, as well as more than 250 sessions under the "X" program in the S/X/Ka bands, were conducted with the MDBE's participation.

4 Conclusions

Experimental operation of this system at the Svetloe Observatory has shown that, in terms of its parameters and characteristics, the MDBE surpasses the DAS and the existing backends previously used on the radio telescopes of the Quasar VLBI Network. The MDBE provides signal conversion for both broadband and narrowband registration during VLBI observations, making it possible to conduct radar observations of the Moon. The use of the MDBE will allow in the future abandonment of separate recording systems for radiometric and spectral observations. The MDBE provides observations in various modes without replacing equipment and allows improvement of the obtained results.

Table 1 Basic parameters of the MDBE.

Number of DSP units	Up to 12
ADC sample rate	4096 MSPS
Input bandwidth	2 GHz
Full scale input power	0 dBm (1 GHz sine wave, open attenuator)
DSP unit output	10 GbE SFP+ module, 40 GbE QSFP module
DSP unit core chip	FPGA: 900 multipliers, 400K flip-flops, embedded ARM Cortex-A9 processor
Memory	512 MB (DDR3), microSD card
Control interface	10/100/1000 Ethernet, fiber or copper
Debug interface	USB-JTAG and USB-UART bridge
Input synch. signals	5, 10 or 100 MHz, 2 × 1PPS
Weight	15 kg (eight channel version)
Size	48 × 35 × 18 cm (L × W × H)
Power supply	220 VAC, 440 W

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