VLBI2010 Receiver Back End Comparison

Bill Petrachenko
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Introduction.

VLBI2010 requires a receiver back-end to convert analog RF signals from the receiver front end into channelized digital data streams to be recorded or transmitted electronically. The back end functions are typically performed in two steps: conversion of analog RF inputs into IF bands (see Table 2), and conversion of IF bands into channelized digital data streams (see Tables 1a, 1b and 1c). The latter IF systems are now completely digital and generically referred to as digital back ends (DBEs).

In Table 2 two RF conversion systems are compared, and in Tables 1a, 1b, and 1c nine DBE systems are compared. Since DBE designs are advancing rapidly, the data in these tables are only guaranteed to be current near the update date of this document.

DBE Comparison Table (Tables 1a, 1b, 1c)

In Tables 1a, 1b and 1c nine DBEs are compared. These include:

- ***Roach-based Digital Back End (RDBE***): This DBE is the joint product of Haystack Observatory and the National Radio Astronomy Observatory (NRAO) with Haystack being responsible for the Polyphase Filter Bank (PFB) personality and NRAO for the Direct Digital Converter (DDC) personality. In the near term additional development work on the PFB personality continues at Haystack to add features such as PCAL detection and GNSS tick offset monitoring and to make a transition from real to complex mode and from Mk5B to VDIF output. In the longer term a bandwidth increase from 512 to 1024 MHz is planned in order to raise the VLBI2010 compliance from *Half* to *Full*. More information can be obtained from:
    - Arthur Niell, Haystack Observatory, aniell@haystack.mit.edu
    - Jon Romney, NRAO, jromney@aoc.nrao.edu
- ***DBBC2010-8L8C, DBBC2010-8H8C:*** This is an extension of the familiar DBBC2 developed by Gino Tuccari at INAF with boards added to handle the increased number of IF inputs specified for VLBI2010. The 8L8C version handles 512 MHz IF inputs, while the 8H8C version handles 1024 MHz IF inputs. More information can be obtained from:
    - Gino Tuccari, INAF/IRA, g.tuccari@ira.inaf.it
- ***CDAS-DDC and CDAS-PFB***: These have been developed by a team led by Xiuzhong Zhang at Shanghai Astronomical Observatory. Work continues on both systems to improve compatibility with VLBI2010. In particular plans exist to increase the efficiency of the CDAS-DDC for

VLBI2010. There is no planned commercial availability of the CDAS, but manufacture of a small number of units for use outside China may be possible. More information can be obtained from:

  - Xiuzhong Zhang, Shanghai Astronomical Observatory, xzhang@shao.ac.cn

- ***ADS3000+:*** The ADS3000+ is a joint development of NICT, JAXA/ISAS, and COSMO RESEARCH Corp. It is a DDC based system but has modes compatible with VLBI2010 if enough systems are used. More information can be obtained from:
  - Hiroshi Takeuchi, JAXA, takeuchi@isas.jaxa.jp
  - Kazuhiro Takefuji, NICT, takefuji@nict.go.jp
- ***Russian Broadband Acquisition System (BRAS):*** The BRAS DBE is being developed at IAA by Evgeny Nosov. It outputs the entire 512 MHz input IF as a single 512 MHz wide channel. More information can be obtained from:
  - Evgeny Nosov. E84@mail.ru
- ***JPL DBE:*** This DBE is being developed at JPL. It is mainly intended to support JPL VLBI activities related to deep space tracking in the Deep Space Network (DSN) including support of the X/Ka CRF. It has a unique two step channelization process where a 500 MHz input band sampled at 1280 MHz uses a PFB to produce 8 160 MHz bands which are further subdivided using DDC to channels with programmable bandwidths of less than 32 MHz. More information can be obtained from:
  - Eric Clark, JPL, jec@jpl.nasa.gov
- **XCube StreamX-VLBI (VLBI-In-a-Box):** This is a commercial system adapted to VLBI with support from NRAO and CSIRO and others. This system is a digital backend and data recorder in a single box. The system is configurable in terms of number of IO channels and FPGA and GPU compute resources. The base system has 4 bands at 512MHz with a PFB filter bank dividing it to 16, 32MHz bands. The system also has a RAW mode, and a GPU for software processing. It can be extended to 8 Channels with an additional sampler card. The recorder part can operate up to 24Gbit/s recording to removable media, or send data over Ethernet. As a recorder the StreamX VLBI is compatible with other DBE. A DDC mode and a larger PFB, 16MHz bands, are planned. In addition, data monitoring, real-time spectrometer and more are available. More information can be obtained from:
  - Mikael Taveniku, mtaveniku@x3-c.com
- It is possible that other DBEs exist that might be applicable to VLBI2010. However, at the time of preparation of this comparison, data were only available for these nine DBE's.

Heading descriptions:

- ***VLBI2010 compliant***: DBEs were qualified as either *Half* or *Full* VLBI2010 compliant. *Half* compliant implies at least eight IF inputs of 512 MHz, at least eight 32 MHz channel outputs per IF, and a total output data rate of at least 8 Gbps. *Full* implies at least eight IF inputs of 1024 MHz (could be 2*512 MHz), at least sixteen 32 MHz channels per IF, and a total output data rate of at least 16 Gbps.
- ***IF's/Unit.*** This is the number of IF inputs per unit. It is one of the factors that determine the number of units needed per VLBI2010 system.
- ***Units/VLBI2010.*** This the number of units required for a VLBI2010 system (either *Half* or *Full*).
- ***Sampler Resolution (bits).*** This is the number of bits resolution per sample.
- ***Input Gain Set.*** This is either *internal* or *external* depending on whether or not digitally controlled variable attenuators are built into the system. [Note: In the case of the ADS3000+, the gain setting is done inside the FPGA by selecting the best 4 of 8 bits to continue in the processing.]
- ***Sampler Bandwidth (GHz).*** This is the maximum frequency that can be input into the sampler without significant degradation. It determines the highest Nyquist zone that can be used.
- ***Input Bandwidth (GHz).*** This is the bandwidth of each Nyquist zone, i.e. the bandwidth that is actually processed.

The next three inputs are applicable only for systems with PFB personalities. If a PFB personality does not exist, they are left blank.

- ***PFB – Channel Bandwidth (MHz).*** This is the bandwidth of each output channel.
- ***PFB – Max # of channels per IF.*** This is the maximum number of output channels. This should normally be calculated according to Input bandwidth/PFB Channel bandwidth.
- ***PFB – Channel Selection.*** This refers to the degree of flexibility in selecting channels to be routed to the output.

The next three inputs are applicable only for systems with DDC personalities. If a DDC personality does not exist, they are left blank.

- ***DDC – Channel Bandwidth (MHz).*** This is the bandwidth of each output channel.
- ***DDC – # per unit.*** This is the number of DDC output channels per unit.
- ***DDC – Frequency resolution.*** This refers to the degree of flexibility in selecting channels to be routed to the output.
- ***Requantization Threshold.*** How many bits per output sample.
- ***Real/Complex.*** Is the output available in real or complex format or both.
- ***PCAL/Total Power.*** Is there a Pcal and/or total power function.
- ***Total Data Rate.*** This is the total data rate for all units making up the VLBI2010 system.
- ***Output layer.*** VSI-H or 10GE

- ***VDIF.*** Is VDIF output format provided? [Note. In the case of the DBE's with VSI-H outputs it is possible to generate VDIF output if these DBE's are interfaced with a VDIF-compatible recorder of 10GE converter (e.g. K5 recorder).]
- ***Availability.*** Is the DBE commercially available?
- ***Availability Date.*** At what date will the DBE be commercially available
- ***Upgradable.*** Can the VLBI2010 DBE be produced by upgrading a previous version of the DBE.
- ***Cost.*** Separated into the cost for a *Full* and/or *Half* system

Table 1a	***RDBE***	***DBBC2010-8L8C***	***DBBC2010-8H8C***
VLBI2010 Compliant	Half	Half	Full
IF's/Unit	2	8	8
Units/VLBI2010	4	1	1
Sampler resolution (bits)	8	8	10 at ADC/ 8 at FPGA
Input Gain Set	Internal	Internal	Internal
Sampler BW (MHz)	0-1536	0-2200	0-3500
Input BW (MHz)	512	512	1024
PFB - Channel BW (MHz)	32	32	32/4
PFB – Max # channels per IF	15 (16 per unit)	15 (128 per unit)	31/15 (256/128 per unit)
PFB - Channel selection	Flexible	Flexible	Flexible
DDC - Channel BW (MHz)	1/2/4/8/16/ 32/64/128	1/2/4/8/16	1/2/4/8/16
DDC - # per unit	4/4/4/4/4/4/2/1	32 UL	32 UL
DDC – Frequency resolution (Hz)	250K (15.625K)	10K (1024e6/2^31)	10K (2048e6/2^31)
Requantization threshold	2-bit	1-, 2-, or 4-bit	1-, 2-, or 4-bit
Real/Complex	Yes/Yes(2013)	Yes/Yes	Yes/Yes
Pcal/Total Pwr	Yes(2013)/Yes	Yes/Yes	Yes/Yes
Data Rate/Unit (Gbps)	2	16	32
Total Data Rate (Gbps)	8	16	32
Output Layer	10GE	10GE/VSI-H	10GE/VSI-H
VDIF	(2013)	Yes	Yes
Availability	Commercial	Commercial	Commercial
Availability Date	Now	Now	Now
Upgradable	Yes	Yes	Yes
Cost/Unit	$18K	84.7K€	98.6K€
Cost ***(Half VLBI2010)*** ***(Full VLBI2010)***	 $72K -	 84.7K€ -	 - 98.6K€

Table 1b	***CDAS-DDC (China)***	***CDAS-PFB (China)***	***ADS3000+ (Japan)***
VLBI2010 Compliant	Yes (VSI-H)	Yes (VSI-H)	Yes (VSI-H)
IF's/Unit	4	2	4
Units/VLBI2010	4(half)/8(full)	4(half)/8(full)	4(half)/8(full)
Sampler resolution (bits)	8	8	10 at ADC/8 at FPGA/ 4 for processing
Input Gain Set	Internal	External	Inernal (see note)
Sampler BW (MHz)	50 -1024	50 -1024	0-2500 (-3dB@1800)
Input BW (MHz)	512	512	4 x 512 2 x 1024 1 x 2048
PFB - Channel BW (MHz)	-	32 /64	-
PFB – Max # of channels per IF	-	15/7	-
PFB - Channel selection	-	All	-
DDC - Channel BW (MHz)	1/2/4/8/16/32	-	4/8/16/32
DDC - # of channels per unit	16	-	16
DDC – Frequency resolution (Hz)	1 (10K)	-	1
Requantization threshold	1-,2- or 4-bit	1- or 2-bit	2- or 4-bit
Real/Complex	Yes/No	Yes/No	Yes/Yes
Pcal/Total Pwr	yes/yes	No/yes	no/no
Data Rate/Unit (Gbps)	2 (VLBI2010 mode)	4	2 (VLBI2010 mode)
Total Output Rate (Gbps)	8(half)/16(full)	16(half)/32(full)	8(half)/16(full)
Output Layer	VSI-H (10GE soon)	VSI-H (10GE soon)	VSI-H (10GE soon)
VDIF	With converter	With converter	With converter
Availability	Small number	Small number	Commercial
Availability Date	Now	Now	Now
Upgradable	Yes	Yes	Yes
Cost/Unit	$50K	$10K	$40K
Cost ***(Half VLBI2010)*** ***(Full VLBI2010)***	 $200K $400K	 $40K $80K	 $150K $285K

Table 1c	***BRAS (Russia)***	***JPL DBE (USA)***	***XCube (USA)***
VLBI2010 Compliant	Half	Half	Half/Full
IF's/Unit	8	2	4/8(2013)
Units/VLBI2010	1	4	1 or 2
Sampler resolution (bits)	8	10 (8 used) (@1280 Gsps)	8 (10 planned)
Input Gain Set	Internal	Internal	External
Sampler BW (MHz)	0-1600	0-2000	50-1600
Input BW (MHz)	512	500	512
PFB - Channel BW (MHz)	512	160 for internal use only	32/16(2013)
PFB - Max # of channels per IF	1	8 for internal use only	16/32(2013)
PFB - Channel selection	NA (only one 512 MHz band/IF)	All - but for internal use only	All – selectable IF
DDC - Channel BW (MHz)	-	32 or less, programmable	(2013)
DDC - # of channels per unit	-	16 complex or 32 UL	
DDC – Frequency resolution (Hz)	-	-	
Requantization threshold	2- to 8-bits	-	2-bit
Real/Complex	Yes/No	Yes/Yes	Yes/No(?)
Pcal/Total Pwr	Yes/no	Yes/Yes	Software Programmable
Data Rate/Unit (Gbps)	8	2	8/16(32)
Total Output Rate (Gbps)	8	8	8/(16)
Output Layer	10GE	10GE	Disk/10GE
VDIF	-	-	(2013, software)
Availability	Not commercial	Not commercial	Commercial
Availability Date	Mid-2013	Oct 2013	Now
Upgradable	NA	NA	NA
Cost/Unit	NA	NA	$50/70K (incl. recorder)
Cost			
(Half VLBI2010)	NA	NA	$50/$70K (incl. recorder)
(Full VLBI2010)	NA	NA	$100K/($140K)

Flexible Down Converter Comparison Table (Table 2)

In Table 2, two flexible down-converters are compared. These include:

- ***UpDown Converter (UDC)***: This flexible down-converter was designed by Alan Rogers at Haystack Observatory. It is a traditional analog design. More information can be obtained from:
    - AEE Rogers, Haystack Observatory arogers@haystack.mit.edu
        - See Mk5 Memo's 59 and 70.
- ***DBBC3:*** This flexible down-converter was designed by Gino Tuccari. It is a fully digital design with a high speed input sampler. More information can be obtained from:
    - Gino Tuccari, INAF/IRA, g.tuccari@ira.inaf.it

Heading descriptions:

- ***VLBI2010 compliant***: VLBI2010 flexible down-converters need to handle a pair of 2-14 GHz RF inputs (assumed to be both polarizations of the same signal), down-converting, with sub-MHz resolution, four pairs of 1024 MHz (or 512 MHz for *Half* compliant) bands to a Nyquist zone for sampling.
- ***Units/VLBI2010.*** This is the number of units required for a VLBI2010 system, i.e. the number of units needed to down-convert four pairs of bands.
- ***Sampler Resolution (bits).*** This is the number of bits resolution per sample.
- ***Input range (GHz).*** The input range is assumed to be 2-14 GHz for VLBI2010.
- ***BW per Output Band(GHz).*** This is assumed to be 512 MHz for *Half VLBI2010* compliant and 1024 MHz for *Full* compliant.
- ***Total # of outputs per RF input.*** This needs to be at least 4 for VLBI2010.
- ***Band selection step size.*** This needs to be at least sub-MHz, but for full compatibility with the original Haystack UpDown Converter this needs to be a sub-multiple of 0.4 MHz.
- ***Channel formation.*** Analog or digital.
- ***Total output rate.*** This is only meaningful for digital systems.
- ***Output layer.*** This is only meaningful for digital systems.

Table 2	***Up-Down Converter (UDC)***	***DBBC3***
VLBI2010 Compliant	nearly (input range and output BW need adjusting)	Full
RF Inputs/Unit	2	4
Units/VLBI2010	4	1
Sampler resolution (bits)	Analog	8 @ 28 Gsps
Input Range (GHz)	1-12 (2-14 planned)	0-14
BW per Output Band(MHz)	512 (1024 planned)	512/1024
Total # outputs per RF input	4	8
Band selection step size (MHz)	0.4	0.01
Channel Formation	Analog	DDC
Total Output Rate (Gbps)	Analog	224 per IF
Output Layer	Analog	40/100 GE
Commercially Available	Possible	orders possible in 2013
Availability Date	TBD	about 8 months after order
Upgradable	Yes	Yes
Cost/Unit	$20-25K USD	30-35K€
Cost (Full VLBI2010)	$80-100K USD	30-35K€